IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Number	09/826693	**Docket Number**	MIPS.0172-00-US
Filed	04/04/01	**Group Art Unit**	2185
Examiner	REGINALD G. BRAGDON	**Customer No.**	23669
Application Title	SYSTEM AND METHOD FOR DATE CACHE BYPASSING IN A STREAM PROCESSING UNIT FOR A MULTI-STREAMING PROCESSOR		
First Named Inventor	MARIO D. NEMIROVSKY		

FACSIMILE COVER SHEET

To: **Commissioner for Patents - Central Fax Number**
Fax Number: **571-273-8300**

From: **HUFFMAN PATENT GROUP, LLC**
Fax Number: **(661) 460-1986**

Pages: **35 (including this cover sheet)**

Dear Sir:

Please accept the attached correspondence for the above-identified matter. I hereby certify under 37 CFR 1.8 that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office on the date of signature shown below.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

/Richard K. Huffman/

By: _____

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Tel: (719) 575-9998

02/01/2006

Date: _____

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LETTER TO EXAMINER

VIA FACSIMILE: 571-273-8300

Mail Stop **AMENDMENT**
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In the Office Action mailed 01/25/2006, the Examiner noted that citation AP, "Kessler et al.," from the Information Disclosure Statement submitted on 04/21/2005 was not considered because the copy of the document was not legible. The undersigned can only speculate that an illegible copy of the document was produced within the PTO. Accordingly, another copy of that portion of the submittal is attached hereto.

In addition, the undersigned notes that citation AG, "ESA/390 Principles of Operation," from the same Information Disclosure Statement, was not signed off by the Examiner. Perhaps the copy of that portion of the submittal was rendered illegible during copying as well. Accordingly, another copy of citation AG is provided herewith and follows of citation AP.

Respectfully submitted,
HUFFMAN PATENT GROUP, LLC

/Richard K. Huffman/

By _____

RICHARD K. HUFFMAN
Registration No. 41,082
(719) 575-9998

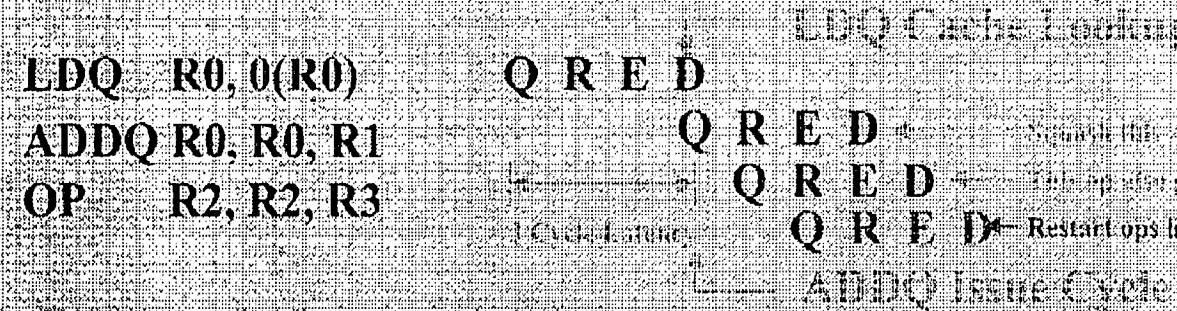
02/01/2006

Date: _____

COMPAQ
The Alpha 21264 Microprocessor:
Out-of-Order Execution at 600 Mhz
R. E. Kessler
COMPAQ Computer Corporation
Shrewsbury, MA
AP

COMPAQ

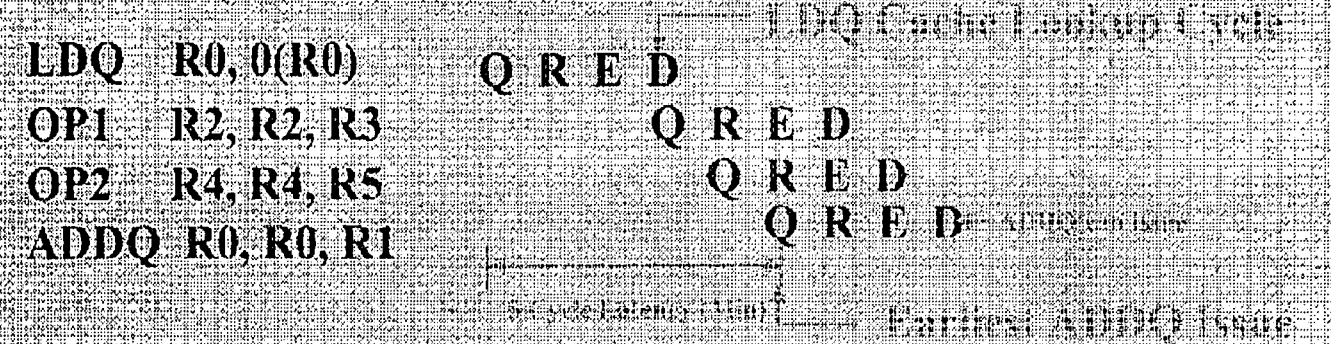
Low-latency Speculative Issue of Integer Load Data Consumers (Predict Hit)



- **When predicting a load hit:**
  - The ADDQ issues (speculatively) after 3 cycles
  - Best performance if the load actually hits (matching the prediction)
  - The ADDQ issues before the load hit/miss calculation is known
- **If the LDQ misses when predicted to hit:**
  - Squash two cycles (replay the ADDQ and its consumers)
  - Force a "mini-replay" (direct from the issue queue)

COMPAQ

Low-latency Speculative Issue of Integer Load Data Consumers (Predict Miss)



- **When predicting a load miss:**
  - The minimum load latency is 5 cycles (more on a miss)
  - There are no squashes
  - Best performance if the load actually misses (as predicted)
- **The hit/miss predictor:**
  - MSB of 4-bit counter (hits increment by 1, misses decrement by 2)

Title: ESA/390 Principles of Operation
Document Number: SA22-7201-01
Build Date: 09/23/93 08:36:13 Build Version: 1.2
Book Path: /home/webapps/epubs/ludocs/book/dz9ar001.boo

CONTENTS Table of Contents

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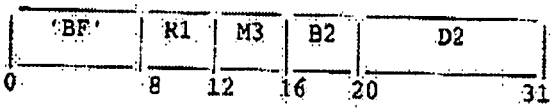
7.5.31 INSERT CHARACTERS UNDER MASK

ICM R1,M3,D2(B2) [RS]



Bytes from contiguous locations beginning at the second-operand address are inserted into general register R1 under control of a mask.

The contents of the M3 field are used as a mask. These four bits, left to right, correspond one for one with the four bytes, left to right, of general register R1. The byte positions corresponding to ones in the mask are filled, left to right, with bytes from successive storage locations beginning at the second-operand address. When the mask is not zero, the length of the second operand is equal to the number of ones in the mask. The bytes in the general register corresponding to zeros in the mask remain unchanged.

The resulting condition code is based on the mask and on the value of the bits inserted. When the mask is zero or when all inserted bits are zeros, the condition code is set to 0. When the inserted bits are not all zeros, the code is set according to the leftmost bit of the storage operand: if this bit is one, the code is set to 1; if this bit is zero, the code is set to 2.

When the mask is not zero, exceptions associated with storage-operand access are recognized only for the number of bytes specified by the mask. When the mask is zero, access exceptions are recognized for one byte at the second-operand address.

Resulting Condition Code:

0 All inserted bits zeros, or mask bits all zeros
1 Leftmost inserted bit one
2 Leftmost inserted bit zero, and not all inserted bits zeros
3 --

Program Exceptions:

- Access (fetch, operand 2)

Programming Notes:

1. Examples of the use of the INSERT CHARACTERS UNDER MASK instruction are given in Appendix A, "Number Representation and Instruction-Use Examples."

2. The condition code for INSERT CHARACTERS UNDER MASK is defined such that, when the mask is 1111, the instruction causes the same condition code to be set as for LOAD AND TEST. Thus, the instruction may be used as a storage-to-register load-and-test operation.

3. INSERT CHARACTERS UNDER MASK with a mask of 1111 or 0001 performs a function similar to that of a LOAD (L) or INSERT CHARACTER (IC) instruction, respectively, with the exception of the condition-code setting. However, the performance of INSERT CHARACTERS UNDER MASK may be slower.

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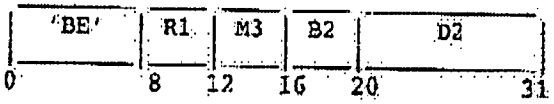
7.5.70 STORE CHARACTERS UNDER MASK

STCM R1,M3,D2(B2) [RS]



Bytes selected from general register R1 under control of a mask are placed at contiguous byte locations beginning at the second-operand address.

The contents of the M3 field are used as a mask. These four bits, left to right, correspond one for one with the four bytes, left to right, of general register R1. The bytes corresponding to ones in the mask are placed in the same order at successive and contiguous storage locations beginning at the second-operand address. When the mask is not zero, the length of the second operand is equal to the number of ones in the mask. The contents of the general register remain unchanged.

When the mask is not zero, exceptions associated with storage-operand accesses are recognized only for the number of bytes specified by the mask.

When the mask is zero, the single byte designated by the second-operand address remains unchanged; however, on some models, the value may be fetched and subsequently stored back unchanged at the same storage location. This update appears to be an interlocked-update reference as observed by other CPUs.

Condition Code: The code remains unchanged.

Program Exceptions:

- Access (store, operand 2)

Programming Notes:

1. An example of the use of the STORE CHARACTERS UNDER MASK instruction is given in Appendix A, "Number Representation and Instruction-Use Examples."

2. STORE CHARACTERS UNDER MASK with a mask of 0111 may be used to store a three-byte address, for example, in modifying the address in a CCW.

3. STORE CHARACTERS UNDER MASK with a mask of 1111, 0011, or 0001 performs the same function as STORE, STORE HALFWORD, or STORE CHARACTER, respectively. However, on most models, the performance of STORE CHARACTERS UNDER MASK is slower.

4. Using STORE CHARACTERS UNDER MASK with a zero mask should be avoided since this instruction, depending on the model, may perform a fetch and store of the single byte designated by the second-operand address. This reference is not interlocked against accesses by channel programs. In addition, it may cause any of the following to occur for the byte designated by the second-operand address: a PER storage-alteration event may be recognized; access exceptions may be recognized; and, provided no access exceptions exist, the change bit may be set to one. Because the contents of storage remain unchanged, the change bit may or may not be one when a PER storage-alteration event is recognized.

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